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REMARKS

The objections and rejections of claims 1-7 contained in the Office Action dated 3/08/2006 are respectfully traversed.

Claims 1-7 are in the case, no new claims are added and none are canceled.

The Examiner pointed out that the pages in the application were misnumbered and suggested renumbering the pages. During a telephone conference with the Examiner on 5/30/2006 it was suggested that an Examiner's amendment could be used to correct the page numbers, but that the final patent if allowed would not bear the same pages numbers in any event, and that the pages can be referenced in a non-confusing manner (e.g., second page 2). Therefore nothing affected page numbering is presented in this response.

The Examiner pointed out several other typographical errors which are hereby corrected.

Also, the paragraph on the second page 3, line 20-24, is hereby edited to be more clear. This edit make clear that the many assemblies and constructions are known in the art, but preferred embodiments on the present invention integrate them on a single chip with no added wiring, which the prior art required. No new matter is added as the substance of this paragraph is repeated throughout the original application.

The Examiner objected to wording informalities in Claims 1 and 6 that are hereby corrected.

Claims 1-3, and 6 were rejected under 35 USC 102(b0 as being anticipated by US Pat. No. 6,312,846 to Marsh (Marsh).

Marsh, as pointed out on the first page 2, lines 18, of the original application is disclosing building ***his structure on a wafer containing many chips***. The present invention is directed to building an integrated power system on a single chip. The disadvantage of the Marsh disclosure, as discussed in the original application, see first page 2, lines 27-31, is that Marsh requires additional wiring (most likely wire bonds) between the individual chips on the wafer. The present invention requires none.

Marsh, by my reading, does not disclose exactly how the interconnections are made between the chips on his wafer, but the well known use of wire bonds (similar to those used connecting to a chip in an IC package) may be assumed. But that task would require additional steps that are not performed using the present invention. Also, the area between chips on a wafer is not used. See Marsh's FIG. 1, where the individual chips 12, 15 and others hold the functional parts as shown in Marsh's FIG. 8. See Marsh's column 5, lines 47-51, where FIG. 8 is described "some of the possible circuits that may be integrated along with a micro-controlled onto ***the semiconductor wafer.***" Emphasis added. These functional parts are integrated but on separate chips with interconnections necessary between the chips.

Marsh is constructing a system on different chips on the same wafer, but he is not suggesting placing the assemblies on the same chip as in the present invention.

Claims 4, 5, and 7 were rejected under 35 USC 103(a) as being unpatentable over Marsh in view of the Applicant's Background section. Since Marsh is using separate chips for separate function, Marsh may construct a power transistor in a separate chip. But marsh does not suggest forming a power transistor on the same chip with other as-

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semblies. Also, since Marsh is interconnecting chips on the same wafer, if Marsh added a chip (or added to a chip) bearing power transistors with connections on either side of the power transistor chip (as in claim 5) it would be very hard indeed to make an electrical connections to the bottom of the entire wafer, and Marsh does not suggest any such construction, nor is there any reference disclosing such a construction known to Applicant.

As made clearer by the present editing of paragraph on the second page 3, lines 20-24, the subassemblies are known, but placing them on one chip is not known.

It is respectfully requested that Marsh be removed as a 102(b) reference in this case, and a Notice of Allowance be issued.

Please charge any additional fee occasioned by this paper to our Deposit Account No. 03-1237.

Respectfully submitted,

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